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Analytical modeling of energy quantization effects in nanoscale mosfets

Amit Chaudhry[1,*], Jatindra Nath Roy[2]

[1]*Faculty of University Institute of Engineering and Technology, Panjab University, Chandigarh, India.*
[2]*Solar Semiconductor Private Limited, Hyderabad, India.*

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Abstract

In this paper, we have studied and developed an analytical model for the inversion layer quantization in nano-metal oxide semiconductor field effect oxide (MOSFET) using the variation approach. Explicit surface potential solutions have been used in the model to accurately model the inversion layer quantization. Capacitance/voltage and Drain voltage/current models in ultra thin oxide MOSFETs have been studied using charge sheet approximation. Drain induced barrier lowering (DIBL) and mobility reduction effects are included in the model developed and hence extended to nanometer scale. Results predict that the inversion layer quantization results in a reduction in drain current and degradation of gate capacitance. The results match closely with the BSIM 5 models proving the accuracy of the model.

Keywords: Inversion layer quantization; DIBL; BSIM; CMOS.
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1. Introduction

MOSFET modeling is facing difficulties to achieve accurate description of extremely scaled down devices. The reason is that many complicated new phenomena are arising which are not easy to describe. One such phenomenon arising out of down scaling the MOSFET is the failure of classical physics at nanometer scale. As Complementary Metal Oxide Semiconductor (CMOS) technology scales down aggressively, it approaches a point, where classical physics is not sufficient to explain the behavior of a MOSFET. Due to extremely thin oxide and high doping concentration very high electrical fields at the oxide/substrate interface occur. This results in the charge carriers occupying quantized two-dimensional sub-bands which behave differently from the classical three- dimensional case [1]. Simple analytical models of the MOSFETs including quantum mechanical effects (QME) are needed for computer-aided design of digital and analog integrated circuits at nanometer scale containing thousands to millions transistors on a silicon chip. Various

*) For Correspondence; E-mail: amit_chaudhry01@yahoo.com.

electrical parameters of a MOSFET such as capacitance-voltage (C-V) and drain current/voltage (I-V) are affected due to inversion layer quantization. The accurate determination of capacitance-voltage (C-V) at nanometer scale is necessary for describing the overall MOSFET behavior. The C-V analysis for a thick oxide MOSFET is studied classically, but as the gate oxide is reduced to a few angstroms in a sub 100nm MOSFET, the electrical fields at the oxide/substrate are increased to a large value causing discreteness of energy levels. This results in occupancy of high energy levels by the electrons causing reduced inversion charge density at the interface. The classical model suggests a maximum inversion charge density at the oxide/substrate interface. If inversion layer quantization occurs, the electron density diminishes at the interface. Through a gate capacitance model that incorporates the inversion layer quantization effect, a better understanding of the behavior of MOSFETs can be achieved.

Similarly, the drain current needs to be understood under inversion layer quantization conditions. The paper is organized as follows: The paper starts with an overview of the existing MOSFET models which include C-V, I-V and inversion layer quantization at nanoscale. Secondly, study and modeling of inversion layer quantization effect has been done. Thirdly, the capacitance voltage and drain current-voltage analysis has been done and finally the paper ends with conclusion and references.

2. Inversion layer quantization

The nanometer-scale MOSFETs use highly-doped substrate and ultra-thin gate oxides to control short-channel effects such as drain induced barrier lowering (DIBL) and the punch through effect. All these methods used to control short channel effects result in a high electric field in the direction vertical to the silicon/silicon oxide interface. Although the high electric field in the vertical direction can keep the charges in the channel under gate control against the influence of drain potential, it confines the movement of carriers in a narrow potential well existing between the surface potential distribution and the infinite oxide potential. According to Heisenberg principle, the energy of the channel carriers can only take discrete values and not a continuous energy distribution as described by classical device physics. The silicon energy band is composed of six equal energy lobes orienting towards six directions. Every energy lobe has two directions also. One is longitudinal and the other is the transverse direction. So, the electrons present in these two directions have masses $0.916m_o$ and $0.19m_o$ respectively. Let the Si/SiO_2 interface is towards (100) direction. So, the electrons in two lobes along the interface have mass $0.916m_o$ and in the other four lobes have transverse mass $0.19m_o$ along the Si/SiO_2 interface. So, combining these four lobes of transverse mass $0.19m_o$ are grouped together and the other two lobes are grouped together as shown in figure 1. When inversion layer quantization occurs, the electrons reside in lower energy valleys i.e. $0.916m_o$ mass. So, 90% of the electron population is in lower valley having longitudinal mass $0.916m_o$ and transverse mass 0.19m band edge of the silicon conduction band as also given by Heisenberg principle. This causes a significant decrease in the inversion carrier density at a Si/SiO_2 interface in MOSFETs as compared to that of the classical case. Thus, it is important to model accurately the inversion layer quantization effect in a nanoscale MOSFET and understand the relationship between the inversion charge density and the surface potential. All the calculations done in this paper are based on the lower energy valley having longitudinal mass $0.916m_o$ and transverse mass $0.19m_o$.

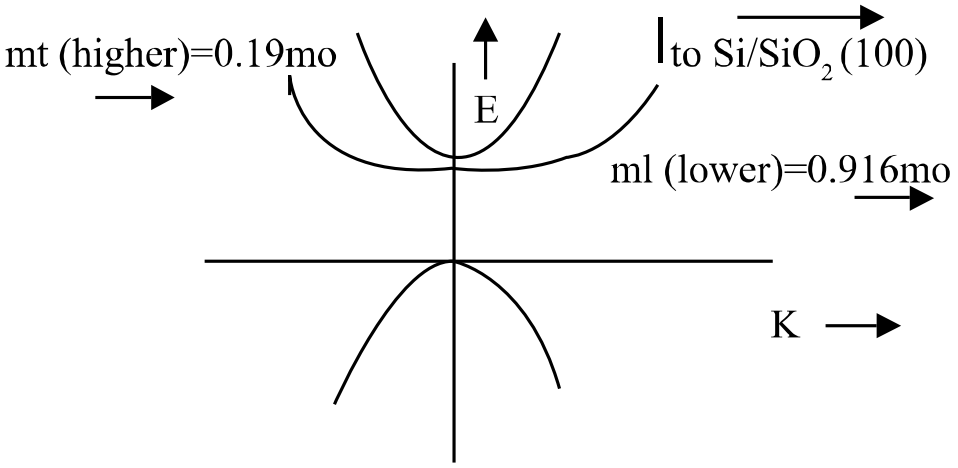

Fig. 1: E-k diagram showing inversion layer lower energy and upper energy and masses in the conduction band valleys.

The research in the area of inversion layer quantization started in the early 1950s. The research[1]-[5] mainly focused on only calculating the inversion charge density in the presence of inversion layer quantization effects using variation approach and triangular well approach in the MOSFET. The use of such techniques required the calculation of surface potentials at the interface of silicon and its oxide. The lack of availability or slow development of surface potential models six decades ago, never allowed the growth of research in the area of modeling QME in MOSFETs. But as the MOSFETs are being scaled down to the nm scale, there is a need to analytically model the inversion layer quantization in nanoscale MOSFETs. Now we discuss the model, simulation and analysis of the inversion layer quantization process in the nanoscale MOSFETs. Solving the Poisson equation in the inverted channel, we get the total charge density, Q_s.

$$Q_s = -(2qN_a\varepsilon_{si}\varepsilon_0)^{1/2}\left[\varphi_s + V_t e^{-2\varphi_f/V_t}\left(e^{\varphi_s/V_t} - 1\right)\right]^{1/2} \tag{1}$$

q is electron charge, ε_{si} is silicon relative permittivity, ε_0 is permittivity of free space, φ_s is surface potential, φ_f is fermi potential, N_a is substrate concentration, and $V_t = kT/q$ is thermal voltage . Similarly, the depletion charge Q_b is approximated as

$$Q_b = -(2\varepsilon_{si}\varepsilon_0 qN_a\varphi_s)^{1/2} \tag{2}$$

Therefore, the inversion charge density Q_{inv} is given by (1) and (2):

$$Q_{\text{inv}} = -\gamma C_{\text{ox}} \left\{ \left[\varphi_s + \frac{kT}{q} \exp\left(\frac{q(\varphi_s - 2\varphi_f)}{kT} \right) \right]^{1/2} - (\varphi_s)^{1/2} \right\} \tag{3}$$

γ is body effect parameter and C_{ox} is oxide capacitance (Fcm^{-2}). The main problem with (3) is that the surface-potential has to be evaluated explicitly in all the regions of inversion and then only, (3) can be solved. An explicit solution has been evaluated in [6]. The wave function solution of the Schrödinger's equation is given by using variation approach [1]:

$$\psi(x) = \frac{b^{3/2} x}{\sqrt{2}} \exp\left(\frac{-bx}{2} \right) \tag{4}$$

b is a constant and given by

$$b = \left[\frac{48\pi^2 m^* q}{\varepsilon_{si} \varepsilon_0 h^2} \left((11/32) Q_{\text{inv}} + Q_{\text{dep}} \right) \right]^{1/3} \tag{5}$$

(5) is then included in the explicit surface potential expression given by [13]:

$$\varphi_s = f + a \tag{6}$$

$$f = \varphi_f + 0.5\varphi_{\text{swi}} - 0.5\left[(\varphi_{\text{swi}} - 2\varphi_f)^2 + 0.0016 \right]^{1/2}$$

$$a = 0.025 \ln\left\{ \left[x - y \left(1 + 100 y^2\right)^{-1/2} \right]^2 (0.16\gamma)^{-2} - 40 f + 1 \right\}$$

$$\varphi_{\text{swi}} = \left[\left(V_{\text{gs}} - V_{\text{fb}} + 0.25\gamma^2 \right)^{1/2} - 0.5\gamma \right]^2$$

And φ_{swi} is the weak inversion surface potential, $x = V_{\text{gs}} - V_{\text{fb}} - f$, and $y = \varphi_{\text{swi}} - f$.

The quantum surface potential is given by

$$\varphi_{\text{sqm}} = 2\varphi_{\text{f}} + \delta\varphi \tag{7}$$

Using the surface potential model (6) in (2) and (3), we can calculate explicitly inversion charge density and depletion charge density. The shift in the surface potential due to inversion layer quantization in the substrate can hence be calculated from (6). Using (5), (6) and (7), the quantum depletion charge density (2) and inversion charge density (3) can be evaluated for quantum mechanical case.

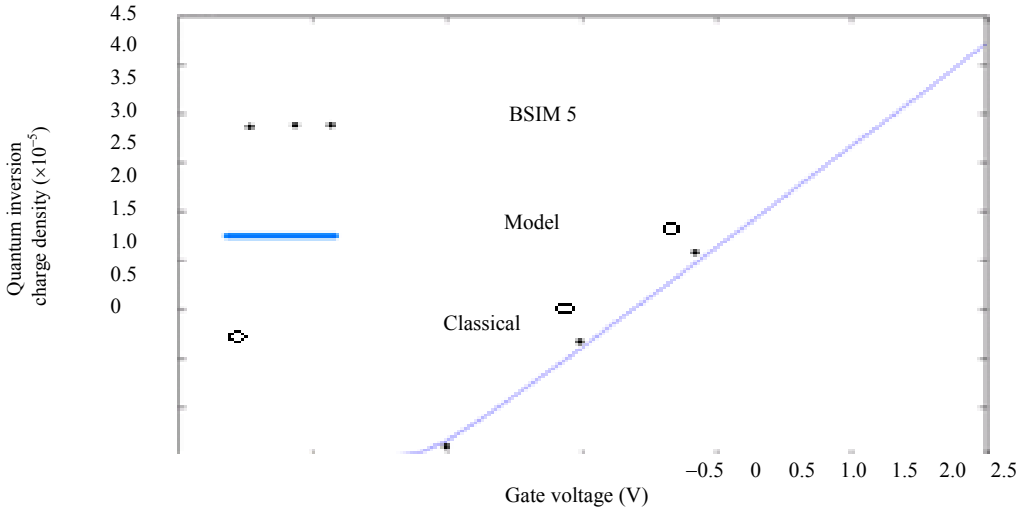

Fig. 2: Simulated results of quantum mechanical inversion charge density with gate voltage under the model parameters: substrate doping $1x10^{18}cm^{-3}$ and oxide thickness 1.5 nm.

The results in figure 2 match quite closely with the BSIM 5 results [7]. The results have been achieved by accurately modeling the shift in the surface potential. The results show that the inversion layer quantization leads to reduced inversion charge density. It has been analytically proved that the classical theory overestimates the value of inversion layer charge density as compared to the quantum mechanical charge density.

3. Gate Capacitance Modeling

Various models [8]-[13] have been reported for the calculation of C-V analysis in the presence of inversion layer quantization, but most of them are numerical in nature. These offer complex solutions and are not suitable for circuit spice simulations. Approximating the inversion charge density for the weak inversion region and strong inversion regions separately, we get after differentiating (3) with surface potential, the weak inversion and strong inversion capacitances. The MOS capacitor under inversion conditions is represented as:

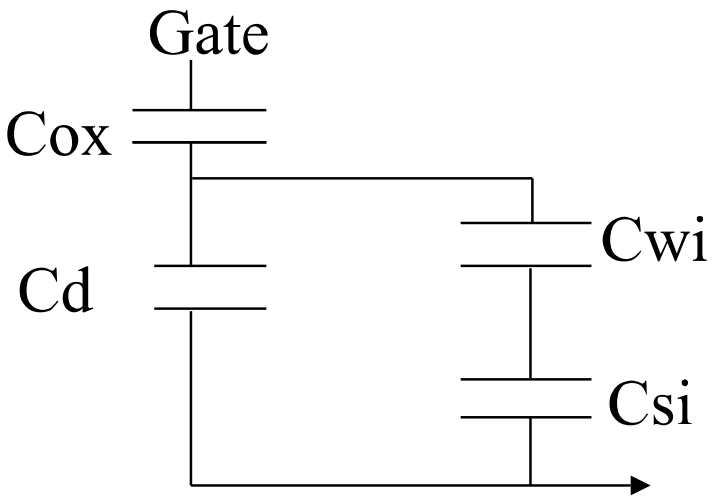

Fig. 3: Equivalent circuit of a MOS capacitor under inversion conditions.

The inversion capacitance is a series combination of weak and strong inversion capacitances.

$$C_i=C_{wi}C_{si}/(C_{si}+C_{wi}) \quad (8)$$

C_i = Inversion capacitance, $C_{wi}=(q/kT)Q_{winv}$ is the weak inversion capacitance, $C_{si}=(q/2kT)Q_{sinv}$ is the strong inversion capacitance. Q_{winv} and Q_{sinv} are the weak inversion and strong inversion charge densities, given by approximating (3) in weak and strong inversion regions. The depletion capacitance C_d is in parallel to the inversion capacitance. Therefore, the total gate capacitance

$$= C_{ox}\,(C_d + C_i) / (C_{ox} + C_d + C_i) \quad (9)$$

C_d is the depletion capacitance obtained by differentiating (2) with the surface potential, $= 0.5\ \gamma_s\ C_{ox}\ \varphi_s^{-1/2}$

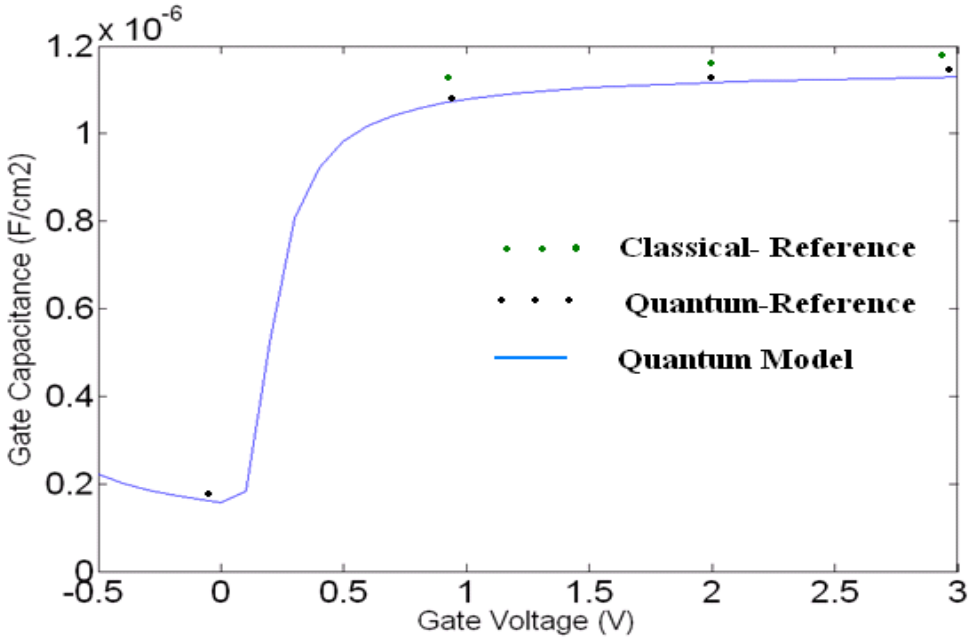

Fig. 4: Simulated results of the quantum gate capacitance. The green dots show the classical gate capacitance and the black dots show the reported [14] quantum mechanical gate capacitance. The blue line shows the modeled quantum mechanical gate capacitance.

4. Drain Current Modeling

In order to evaluate the effect of inversion layer quantization in MOSFET output characteristics, the classical I-V models need to be upgraded. The main consideration lies in the change in the surface potential due to the quantization of continuous energy levels in the substrate and this fact has to be included in the classical model. The model is also extended to the sub 100nm level by adding the short channel effects such as DIBL and mobility reduction.

The drain current above threshold voltage using charge sheet approach as given by [15]

$$I_{ds1}=-\mu C_{ox}(W/L)[(V_{gs}-V_{fb})(\varphi_{sL}-\varphi_{so})-0.5(\varphi_{sL}^{2}-\varphi_{so}^{2})-0.67\gamma(\varphi_{sL}^{3/2}-\varphi_{so}^{3/2})] \quad (10)$$

φ_{sL} and φ_{so} are the surface potentials at drain and source respectively, μ= electron mobility, W and L are the width and channel length respectively, V_{fb} and V_{gs} are flatband and gate to source voltage respectively.
The drain current in sub threshold region as given by [15]

$$I_{ds2}=-\mu\, C_{ox}\,(W/L)V_t[(\varphi_{sL}-\varphi_{so})+\gamma(\varphi_{sL}^{1/2}-\varphi_{so}^{1/2})] \quad (11)$$

V_t is the thermal voltage =kT/q
The total drain current is the summation of (10) and (11).

$$I_{ds}=I_{ds1}+I_{ds2} \quad (12)$$

(13) is upgraded to include the inversion layer quantization by replacing the classical surface potential by the quantum surface potential from (7).

Effective Mobility

The movement of electrons in a MOSFET channel is strongly affected by transverse electric fields. The transverse electric field in the vertical direction, which is caused by applied gate bias, has the effect of decreasing carrier mobility. At the deep sub-micron and nanoscale levels, the transverse fields are very high due to decreased oxide thickness. The degraded mobility is defined as [16]

$$\mu = \mu_o \quad \text{if } V_{gs}<V_T$$
$$= \mu_o/\,\theta\,(V_{gs}-V_T) \text{ if } V_{gs}>V_T \quad (13)$$

μ_o = Low field mobility=0.03m^2/Vs [17], $\theta= \mu_o/2t_{ox}v_{sat}$ is the normal-field mobility degradation factor and v_{sat} = The saturated electron velocity =2.2x10^7m/s, V_T is the classical threshold voltage.

Drain Induced Barrier Lowering (DIBL)

DIBL is an influence of drain potential into substrate surface potential thus lowering the the potential barrier in the substrate with increasing drain-source voltage and causing increasing sub threshold currents. DIBL results in decreased concentration in the substrate due to the depletion caused by the drain potential. To account for the DIBL effect, the substrate concentration ($\mathbf{N_B}$) is replaced with the effective substrate concentration [18] in (2) and (3) i.e.

$$N_B=N_b-(2\varepsilon_o\varepsilon_{si}V_{ds}/qL^2) \quad (14)$$

Putting (13) in (12) and (14) in (2),(3), we get the full quantum mechanical MOSFET model applicable to Sub 100nm geometries. The model has been simulated at effective channel length of 80nm.

5. Results and discussion

Extensive computations have been carried out to estimate the effect of inversion layer quantization on the gate capacitance and drain current in a nanoscale MOSFET. The simulation results for these parameters match quite closely with the reported results, thus proving the accuracy of the analytical model developed. The gate capacitance has been reduced due to the inversion layer quantization due to the reduced inversion charge densities as shown in figure 4. The parameters used for simulation are oxide thickness (t_{ox}) = 3.0nm, substrate doping (N_a) = $3x10^{17}cm^{-3}$. At gate voltage 3.0V and polysilicon doping $1x10^{19}cm^{-3}$, classical gate capacitance is more than $20pF/cm^2$ as compared to quantum mechanical gate capacitance. The drain current also falls due to the reduced inversion charge density in the channel in the presence of inversion layer quantization. At gate voltage of 1.2 V, the drain current falls to around 25% due to inversion layer quantization as shown in figure 4. The modeled quantum mechanical drain current and BSIM 5 results obtained from [7] also match with around 90% accuracy.

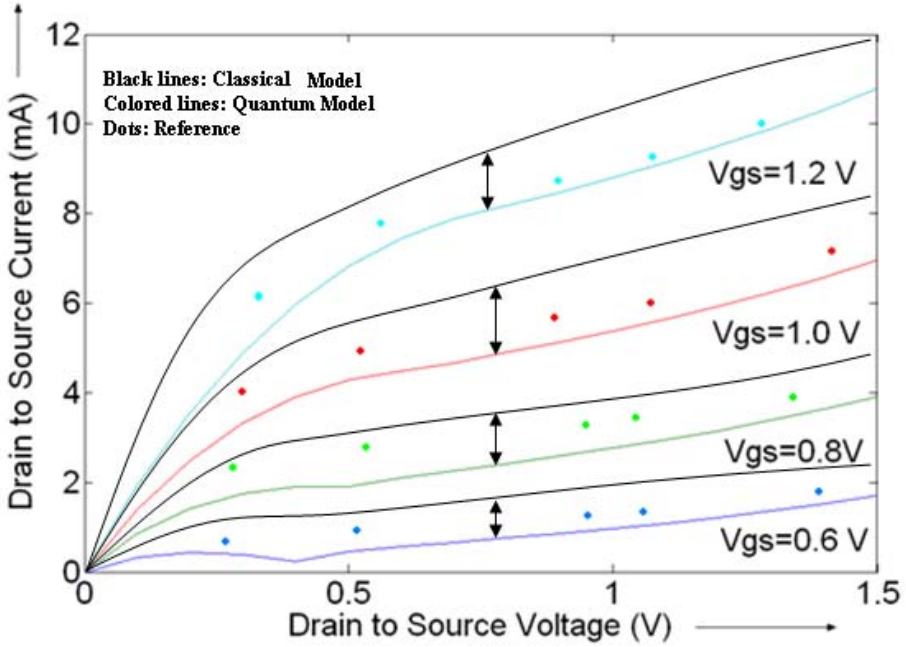

Fig. 4: Simulated drain current at channel length (L)=80nm (Gate length (L_g) =130nm) including inversion layer quantization, poly silicon gate depletion, DIBL and mobility reduction at gate doping N_p =$10^{19}cm^{-3}$ and V_{bs} (body bias) = -0.75. (Empirical fit of 0.03 V has been given to account for polysilicon depletion effect). The colored dots show the reported results [19]. The black lines show the classical modeled results.

6. Conclusion

In this paper, full model has been developed for the QME in the nanometer scale MOSFET. The MOSFET I-V and C-V characteristics in presence of energy quantization effect have been upgraded to include this effect. This model also includes all short channel related effects including mobility reduction and DIBL. The study shows that the drain current decreases due to the energy quantization effect resulting in the significant loss in the drive current. The value calculated by the analytical model and BSIM5 matches closely.

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